BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

WHAT IS CLAIMED IS:

1. An apparatus comprising:

a queue storing a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks, the memory bus incapable of transmitting the plurality of memory transactions simultaneously; and

an arbiter configured to

identify a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction, and

select one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

2. The apparatus of claim 1, further comprising:

a memory controller configured to send the selected memory transaction over the memory bus.

3. The apparatus of claim 1, further comprising:

a queue controller configured to associate with each of the memory transactions a different priority in a set of priorities; and wherein

the arbiter is further configured to select the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

4. The apparatus of claim 3, wherein:

each priority represents an age of a memory transaction.

5. The apparatus of claim 1, wherein:

the arbiter is further configured to generate the bank readiness signals.

6. The apparatus of claim 1, wherein:

the arbiter is further configured to send a memory transaction to a memory bank, clear the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank, and set the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

7. A method comprising:

identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks, the memory bus incapable of transmitting the plurality of memory transactions simultaneously;

identifying a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

8. The method of claim 7, further comprising:

sending the selected memory transaction over the memory bus.

9. The method of claim 7, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein selecting further comprises:

selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

10. The method of claim 9, further comprising:

associating the priorities with the memory transactions based on an age of the memory transactions.

11. The method of claim 7, further comprising:

generating the bank readiness signals.

12. The method of claim 7, wherein generating comprises:

sending a memory transaction to a memory bank;

clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and

setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

13. An apparatus comprising:

means for identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks, the memory bus incapable of transmitting the plurality of memory transactions simultaneously;

means for identifying a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

means for selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

14. The apparatus of claim 13, further comprising:

means for sending the selected memory transaction over the memory bus.

15. The apparatus of claim 13, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein means for selecting further comprises:

means for selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is

destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

16. The apparatus of claim 15, further comprising:

means for associating the priorities with the memory transactions based on an age of the memory transactions.

17. The apparatus of claim 13, further comprising:

means for generating the bank readiness signals.

18. The apparatus of claim 13, wherein means for generating comprises:

means for sending a memory transaction to a memory bank;

means for clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and

means for setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

19. A computer program product, tangibly stored on a computer-readable medium, the product comprising instructions operable to cause a programmable processor to:

identify a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks, the memory bus incapable of transmitting the plurality of memory transactions simultaneously;

identify a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

select one of the memory transactions for transmission over the memory bus based on the bank readiness signals.